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10/667,024	09/18/2003	Kerry Christopher Imming	ROC920030206US1	9121

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EXAMINER	
SAWHNEY, VAIBHAV	
ART UNIT	**PAPER NUMBER**
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/667,024	IMMING ET AL.	
	Examiner	Art Unit	
	VAIBHAV (MANU) SAWHNEY	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8,9 and 11-16* is/are rejected.

7)☒ Claim(s) *6-7, 10, 17-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 12 are rejected under 35 U.S.C. 102(b) as being unpatentable by Witkowski et al. (6,098,110).

As to claim 1, Witkowski et al. show a method of providing a current pointer (TxCurPtr) (Col. 56, lines 25-28; Figs. 11A and 11B) and a stake (TxBasePtr) (Col. 56, lines 25-28; Figs. 11A and 11B) for a packet selected for transmit, maintaining said current pointer for tracking a current position for frame alteration operations in the packet, and maintaining said stake for tracking a start of a current header for frame alteration operations in the packet comprising a transmit base pointer (stake) (is provided and maintained) (TxBasePtr) is a 28-bit pointer to the base (start of the header) of the current transmit packet header, that is, stake pointer for tracking the start of the current header, and another 28-bit transmit current pointer (TxCurPtr) points (provided and maintained) to the current data retrieval location (for tracking the current position of the frame alteration code/instructions) for the corresponding port of the switch (Col. 56, lines 25-28; Figs. 11A and 11B). Witkowski et al. further disclose that each TPI RX FIFO (receive queue) and TPI TX FIFO (transmit queue) of the data

buffers 807a-d is preferably implemented as a circular buffer, with pointers maintained on both sides for writing and reading data (Col. 37, lines 65-67; Col. 38, line 1). Further the FIFO synchronization logic 818 generally operates to synchronize, maintain and update the pointers on both sides of each FIFO to ensure that data is properly written to or read from the appropriate TPI FIFO (Col. 38, lines 2-5). Thus, the pointers are constantly updated and maintained in the switch/network device/processor.

As to claim 12, Witkowski et al. show a computer program product (Fig. 3H shows a flowchart that can be implemented using a computer program product; Fig 5C) of providing a current pointer and a stake for a packet selected for transmit, maintaining said current pointer for tracking a current position for frame alteration operations in the packet, and maintaining said stake for tracking a start of a current header for frame alteration operations in the packet comprising a transmit base pointer (stake) (is provided and maintained) (TxBasePtr) is a 28-bit pointer to the base (start of the header) of the current transmit packet header, that is, stake pointer for tracking the start of the current header, and another 28-bit transmit current pointer (TxCurPtr) points (provided and maintained) to the current data retrieval location (for tracking the current position of the frame alteration code/instructions) for the corresponding port of the switch (Col. 56, lines 25-28; Figs. 11A and 11B). Witkowski et al. further disclose that each TPI RX FIFO (receive queue) and TPI TX FIFO (transmit queue) of the data buffers 807a-d is preferably implemented as a circular buffer, with pointers maintained on both sides for writing and reading data (Col. 37, lines 65-67; Col. 38, line 1). Further

the FIFO synchronization logic 818 generally operates to synchronize, maintain and update the pointers on both sides of each FIFO to ensure that data is properly written to or read from the appropriate TPI FIFO (Col. 38, lines 2-5). Thus, the pointers are constantly updated and maintained in the switch/network device/processor.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 5, 9, 11, 13, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witkowski et al. (6,098,110) In view of Gentry, Jr. (6,356,951).

As to claim 2, Witkowski et al. show all the elements except the method of including the steps of providing frame alteration code instructions to specify an offset from said current pointer. Gentry, Jr. shows the method of including the steps of providing frame alteration code instructions to specify an offset from said current pointer comprising a "success offset" portion of an instruction indicating the number of two-byte units that the pointer (that is, current pointer) is to advance if the comparison between the extracted and test values succeeds. Further, Gentry, Jr. shows a "success instruction" portion of an instruction identifies the next instruction in program 2300 to

execute if the comparison is successful. Further, a "failure offset" and "failure instruction" portions indicate the number of two-byte units to advance the pointer and the next instruction to execute, respectively, if the comparison fails. Although offsets are expressed in units of two bytes (e.g., sixteen-bit words) in this embodiment of the invention, in an alternative embodiment of the invention they may be smaller or larger units (Col. 26, lines 9-22). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the method of Witkowski et al. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

As to claim 3, Witkowski et al. show all the elements except a method wherein said offset is encoded as a 4-bit value for a specified byte 0 to 15 from said current pointer. However, Gentry, Jr. shows a method wherein said offset is encoded as a 4-bit value for a specified byte 0 to 15 from said current pointer comprising a "success offset" portion of an instruction indicating the number of two-byte units that the pointer (current pointer) is to advance if the comparison between the extracted and test values succeeds. Further, Gentry, Jr. shows a "success instruction" portion of an instruction identifies the next instruction in program 2300 to execute if the comparison is successful. Further, a "failure offset" and "failure instruction" portions indicate the number of two-byte units to advance the pointer and the next instruction to execute, respectively, if the comparison fails. Although offsets are expressed in units of two bytes (e.g., sixteen-bit words) in this embodiment of the invention, in an alternative

embodiment of the invention they may be smaller or larger units (thus can include 4 bits offset as well) (Col. 26, lines 9-22). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the method of Witkowski et al. to include any size offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address. In this regard, MPEP 2144.04 shows:

> IV. CHANGES IN SIZE, SHAPE, OR SEQUENCE OF ADDING INGREDIENTS
>
> A. Changes in Size/Proportion
>
> In re Rose , 220 F.2d 459, 105 USPQ 237 (CCPA 1955) (Claims directed to a lumber package "of appreciable size and weight requiring handling by a lift truck" where held unpatentable over prior art lumber packages which could be lifted by hand because limitations relating to the size of the package were not sufficient to patentably distinguish over the prior art.); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976) ("mere scaling up of a prior art process capable of being scaled up, if such were the case, would not establish patentability in a claim to an old process so scaled." 531 F.2d at 1053, 189 USPQ at 148.).
>
> In Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), **the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device**

having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

As to claim 5, Witkowski et al. show all the elements except the method of providing an auto-advance feature of frame alteration code instructions to advance said current pointer.

However, Gentry, Jr. shows the method of providing an auto-advance feature of frame alteration code instructions to advance said current pointer comprising a "success offset" portion of an instruction (auto-advance feature/instruction) indicating the number of two-byte units (arbitrary value) that the pointer (that is the current pointer) is to advance if the comparison between the extracted and test values succeeds. Further, Gentry, Jr. shows a "success instruction" portion of an instruction identifies the next instruction in program 2300 to execute if the comparison is successful. Further, a "failure offset" and "failure instruction" portions indicate the number of two-byte units to advance the pointer and the next instruction to execute, respectively, if the comparison fails. Although offsets are expressed in units of two bytes (e.g., sixteen-bit words) in this embodiment of the invention, in an alternative embodiment of the invention they may be smaller or larger units (Col. 26, lines 9-22). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the method of Witkowski et al. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

As to claim 9, Witkowski et al. show all the elements except the apparatus of providing an auto-advance feature of frame alteration code instructions to advance said current pointer.

However, Gentry, Jr. shows the apparatus (Fig. 1A – host computer system) of providing an auto-advance feature of frame alteration code instructions to advance said current pointer comprising a "success offset" portion of an instruction (auto-advance feature/instruction) indicating the number of two-byte units (arbitrary value) that the pointer (that is the current pointer) is to advance if the comparison between the extracted and test values succeeds. Further, Gentry, Jr. shows a "success instruction" portion of an instruction identifies the next instruction in program 2300 to execute if the comparison is successful. Further, a "failure offset" and "failure instruction" portions indicate the number of two-byte units to advance the pointer and the next instruction to execute, respectively, if the comparison fails. Although offsets are expressed in units of two bytes (e.g., sixteen-bit words) in this embodiment of the invention, in an alternative embodiment of the invention they may be smaller or larger units (Col. 26, lines 9-22). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the apparatus of Witkowski et al. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

As to claim 11, Witkowski et al. show all the elements except the apparatus of including the steps of providing frame alteration code instructions to specify an offset from said current pointer. Gentry, Jr. shows the apparatus (Fig. 1A – host computer system) of including the steps of providing frame alteration code instructions to specify an offset from said current pointer comprising a "success offset" portion of an instruction indicating the number of two-byte units that the pointer (that is, current pointer) is to advance if the comparison between the extracted and test values succeeds. Further, Gentry, Jr. shows a "success instruction" portion of an instruction identifies the next instruction in program 2300 to execute if the comparison is successful. Further, a "failure offset" and "failure instruction" portions indicate the number of two-byte units to advance the pointer and the next instruction to execute, respectively, if the comparison fails. Although offsets are expressed in units of two bytes (e.g., sixteen-bit words) in this embodiment of the invention, in an alternative embodiment of the invention they may be smaller or larger units (Col. 26, lines 9-22). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the apparatus of Witkowski et al. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

As to claim 13, Witkowski et al. show all the elements except the computer program product of including the steps of providing frame alteration code instructions to specify an offset from said current pointer. Gentry, Jr. shows the computer program product (Fig. 1B shows a flow chart that can be implemented by a computer program

product) of including the steps of providing frame alteration code instructions to specify an offset from said current pointer comprising a "success offset" portion of an instruction indicating the number of two-byte units that the pointer (that is, current pointer) is to advance if the comparison between the extracted and test values succeeds. Further, Gentry, Jr. shows a "success instruction" portion of an instruction identifies the next instruction in program 2300 to execute if the comparison is successful. Further, a "failure offset" and "failure instruction" portions indicate the number of two-byte units to advance the pointer and the next instruction to execute, respectively, if the comparison fails. Although offsets are expressed in units of two bytes (e.g., sixteen-bit words) in this embodiment of the invention, in an alternative embodiment of the invention they may be smaller or larger units (Col. 26, lines 9-22). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the method of Witkowski et al. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

As to claim 14, Witkowski et al. show all the elements except a computer program product wherein said offset is encoded as a 4-bit value for a specified byte 0 to 15 from said current pointer. However, Gentry, Jr. shows the computer program product (Fig. 1B shows a flow chart that can be implemented by a computer program product) wherein said offset is encoded as a 4-bit value for a specified byte 0 to 15 from said current pointer comprising a "success offset" portion of an instruction indicating the number of two-byte units that the pointer (current pointer) is to advance if the

comparison between the extracted and test values succeeds. Further, Gentry, Jr. shows a "success instruction" portion of an instruction identifies the next instruction in program 2300 to execute if the comparison is successful. Further, a "failure offset" and "failure instruction" portions indicate the number of two-byte units to advance the pointer and the next instruction to execute, respectively, if the comparison fails. Although offsets are expressed in units of two bytes (e.g., sixteen-bit words) in this embodiment of the invention, in an alternative embodiment of the invention they may be smaller or larger units (thus can include 4 bits offset as well) (Col. 26, lines 9-22). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the method of Witkowski et al. to include any size offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address. In this regard, MPEP 2144.04 shows:

> Further, MPEP 2144.04 shows:
>
> IV. CHANGES IN SIZE, SHAPE, OR SEQUENCE OF ADDING INGREDIENTS
>
> A. Changes in Size/Proportion
>
> In re Rose , 220 F.2d 459, 105 USPQ 237 (CCPA 1955) (Claims directed to a lumber package "of appreciable size and weight requiring handling by a lift truck" where held unpatentable over prior art lumber packages which could be lifted by hand because limitations relating to the size of the package were not sufficient to patentably distinguish over the prior art.); In re Rinehart, 531 F.2d 1048, 189

USPQ 143 (CCPA 1976) ("mere scaling up of a prior art process capable of being scaled up, if such were the case, would not establish patentability in a claim to an old process so scaled." 531 F.2d at 1053, 189 USPQ at 148.).

In Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), **the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.**

As to claim 16, Witkowski et al. show all the elements except the computer program product of providing an auto-advance feature of frame alteration code instructions to advance said current pointer.

However, Gentry, Jr. shows the (Fig. 1B shows a flow chart that can be implemented by a computer program product) of providing an auto-advance feature of frame alteration code instructions to advance said current pointer comprising a "success offset" portion of an instruction (auto-advance feature/instruction) indicating the number of two-byte units (arbitrary value) that the pointer (that is the current pointer) is to advance if the comparison between the extracted and test values succeeds. Further, Gentry, Jr. shows a "success instruction" portion of an instruction identifies the next instruction in program 2300 to execute if the comparison is successful. Further, a "failure offset" and "failure

instruction" portions indicate the number of two-byte units to advance the pointer and the next instruction to execute, respectively, if the comparison fails. Although offsets are expressed in units of two bytes (e.g., sixteen-bit words) in this embodiment of the invention, in an alternative embodiment of the invention they may be smaller or larger units (Col. 26, lines 9-22). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the method of Witkowski et al. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

5. Claims 4, 8, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witkowski et al. (6,098,110) In view of Gentry, Jr. (6,356,951), further in view of Sorokopud (2005/0060418).

As to claim 4, Witkowski et al. show all the elements except the method of providing advance pointer instructions allowing said current pointer and said stake to be advanced an arbitrary number of bytes into the packet.

However, Gentry, Jr. shows the method of providing advance pointer instructions allowing said current pointer to be advanced an arbitrary number of bytes into the packet comprising a "success offset" portion of an instruction (advance pointer instruction) indicating the number of two-byte units (arbitrary value) that the pointer (that is the current pointer) is to advance if the comparison between the extracted and test values succeeds. Further, Gentry, Jr. shows a "success instruction" portion of an

instruction identifies the next instruction in program 2300 to execute if the comparison is successful. Further, a "failure offset" and "failure instruction" portions indicate the number of two-byte units to advance the pointer and the next instruction to execute, respectively, if the comparison fails. Although offsets are expressed in units of two bytes (e.g., sixteen-bit words) in this embodiment of the invention, in an alternative embodiment of the invention they may be smaller or larger units (Col. 26, lines 9-22). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the method of Witkowski et al. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

Sorokopud shows the method of providing advance pointer instructions allowing said stake to be advanced an arbitrary number of bytes into the packet comprising offset value (advanced pointer instruction) that is the offset in bytes from the current header pointer location (stake) (Page 3, paragraph 0037; Fig. 2). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the method of Witkowski et al. and Gentry, Jr. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

As to claim 8, Witkowski et al. show an apparatus of providing a current pointer and a stake for a packet selected for transmit, maintaining said current pointer for tracking a current position for frame alteration operations in the packet, and maintaining

said stake for tracking a start of a current header for frame alteration operations in the packet comprising a transmit base pointer (stake) (is provided and maintained) (TxBasePtr) is a 28-bit pointer to the base (start of the header) of the current transmit packet header, that is, stake pointer for tracking the start of the current header, and another 28-bit transmit current pointer (TxCurPtr) points (provided and maintained) to the current data retrieval location (for tracking the current position of the frame alteration code/instructions) for the corresponding port of the switch (apparatus) (Col. 56, lines 25-28; Figs. 11A and 11B; Fig. 1 - apparatus). Witkowski et al. further disclose that each TPI RX FIFO (receive queue) and TPI TX FIFO (transmit queue) of the data buffers 807a-d is preferably implemented as a circular buffer, with pointers maintained on both sides for writing and reading data (Col. 37, lines 65-67; Col. 38, line 1). Further the FIFO synchronization logic 818 generally operates to synchronize, maintain and update the pointers on both sides of each FIFO to ensure that data is properly written to or read from the appropriate TPI FIFO (Col. 38, lines 2-5). Thus, the pointers are constantly updated and maintained in the switch/network device/processor.

However, Witkowski et al. do not show an apparatus comprising advance pointer instructions for allowing said current pointer and said stake to be advanced an arbitrary number of bytes into the packet.

Gentry, Jr. shows the apparatus (Fig. 1A – host computer system) of providing advance pointer instructions allowing said current pointer to be advanced an arbitrary number of bytes into the packet comprising a "success offset" portion of an instruction (advance pointer instruction) indicating the number of two-byte units (arbitrary value)

that the pointer (that is the current pointer) is to advance if the comparison between the extracted and test values succeeds. Further, Gentry, Jr. shows a "success instruction" portion of an instruction identifies the next instruction in program 2300 to execute if the comparison is successful. Further, a "failure offset" and "failure instruction" portions indicate the number of two-byte units to advance the pointer and the next instruction to execute, respectively, if the comparison fails. Although offsets are expressed in units of two bytes (e.g., sixteen-bit words) in this embodiment of the invention, in an alternative embodiment of the invention they may be smaller or larger units (Col. 26, lines 9-22). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the apparatus of Witkowski et al. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

Sorokopud shows an apparatus (Page 3, paragraph 0032, apparatus - computer type devices) of providing advance pointer instructions allowing said stake to be advanced an arbitrary number of bytes into the packet comprising offset value (advanced pointer instruction) that is the offset in bytes from the current header pointer location (stake) (Page 3, paragraph 0037; Fig. 2). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the apparatus of Witkowski et al. and Gentry, Jr. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

As to claim 15, Witkowski et al. show all the elements except the computer program product of providing advance pointer instructions allowing said current pointer and said stake to be advanced an arbitrary number of bytes into the packet.

However, Gentry, Jr. shows the computer program product (Fig. 1B shows a flow chart that can be implemented by a computer program product) of providing advance pointer instructions allowing said current pointer to be advanced an arbitrary number of bytes into the packet comprising a "success offset" portion of an instruction (advance pointer instruction) indicating the number of two-byte units (arbitrary value) that the pointer (that is the current pointer) is to advance if the comparison between the extracted and test values succeeds. Further, Gentry, Jr. shows a "success instruction" portion of an instruction identifies the next instruction in program 2300 to execute if the comparison is successful. Further, a "failure offset" and "failure instruction" portions indicate the number of two-byte units to advance the pointer and the next instruction to execute, respectively, if the comparison fails. Although offsets are expressed in units of two bytes (e.g., sixteen-bit words) in this embodiment of the invention, in an alternative embodiment of the invention they may be smaller or larger units (Col. 26, lines 9-22). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the method of Witkowski et al. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

Sorokopud shows the computer program product (Fig. 3A shows a flow chart that can be implemented by a computer program product) of providing advance pointer

instructions allowing said stake to be advanced an arbitrary number of bytes into the packet comprising offset value (advanced pointer instruction) that is the offset in bytes from the current header pointer location (stake) (Page 3, paragraph 0037; Fig. 2). Therefore it would have been obvious to one of ordinary skilled in the art at the time of invention to modify the method of Witkowski et al. and Gentry, Jr. to include an offset to be able to move about the memory locations as needed by the instructions as the offset provides an index relative to the base address.

Allowable Subject Matter

6. **Claims 6, 7, 10, 17, and 18 are objected** to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VAIBHAV (MANU) SAWHNEY whose telephone number is 571-272-9738. The examiner can normally be reached on Monday - Friday 07:30AM - 1700 EST, alt. fri. off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KWANG B. YAO can be reached on 571-272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VAIBHAV (MANU) SAWHNEY

KWANG BIN YAO
SUPERVISORY PATENT EXAMINER